

ATTACHMENT A

1. (Amended) Apparatus for providing termination for at least a first pin of a multi-pin component to be mounted in a footprint area of a first surface of a first circuit board, comprising:

a second circuit board, **[configured for mounting]** mounted on a second surface of said first circuit board and **[configured for]** providing a connection to at least a first resistance present thereon;

at least a first conductive pathway from said first surface of said first circuit board to a second surface of said first circuit board to provide access for said at least first pin of said multi-pin component to at least a first location of said second circuit board; and

at least a second conductive pathway, formed at least partially through [using] said second circuit board, from said first location of said second circuit board to said at least a first resistance.

3. (Amended) Apparatus, as claimed in Claim 1, wherein said at least a first resistance is positioned on a surface of said second circuit board.

4. (Amended) Apparatus, as claimed in Claim 1, wherein said at least a first resistance is positioned in an interior region of said second circuit board.

5. (Amended) Apparatus, as claimed in Claim 1, wherein said at least a first resistance is selected from among a surface mount resistor, a printed resistance and a buried resistance.

6. (Amended) Apparatus, as claimed in Claim 1, wherein at least a portion of said at least a first conductive pathway **[includes a pathway using]** comprises a via including a conductive material formed in said first circuit board.

7. (Amended) Apparatus, as claimed in Claim 1, wherein said second circuit board is wholly aligned within at least a portion of the region defined by said footprint.

9. (Amended) Apparatus, as claimed in Claim 8, wherein said second portion of said second circuit board provides at least a portion of a third conductive pathway to a location of said first circuit board outside said footprint.

11. (Amended) Apparatus, as claimed in Claim 1, wherein each of said first and second circuit boards has a thickness and wherein said at least a first conductive pathway and said at least a second conductive pathway have a combined length which is less than the sum of the thickness[es] of said first and second circuit boards.

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## ATTACHMENT B

Cross-reference is made to U.S. Patent Application Serial No. 09/481,139, [Attorney File No. 4103-57393] filed January 11, 2000, incorporated herein by reference.

Please replace the paragraph beginning on page 5, line 19 as follows:

As depicted in Fig. 1, in previous devices a circuit board 112 may have one or more multiple-pin ASICs 114 or similar multi-pin devices mounted thereon. Defining a footprint 115 of the ASIC on the circuit board 112. In many common previous approaches, the underside 116 of the ASIC 114 is provided with an array of solder balls corresponding to ASIC signal, power, ground or other pins. In mounting, the ASIC is positioned such that the solder balls and/or pins are aligned with corresponding pads or the like (only one of which 118 is depicted in Fig. 1). The pads 118 can be provided with printed wires or traces to achieve the desired signal routing, or other electronic connections. In many devices, the array of pins and/or solder balls 122 is relatively dense (such as 1100 or more pins in an area of 1600 mm<sup>2</sup>). In many situations, the ball array or pin array is so dense that it is infeasible to position termination resistors within the ASIC footprint 115. In many previous approaches, a printed wire or other lead 124 is provided to connect a pad 118 (coupled to a pin of the ASIC 114), to a termination resistor 126 which may be positioned outside the footprint 115 and thus may provide a stub [124] having a length [126] 128 sufficiently great to create undesirable effects such as reflection, signal distortion, EMI and the like. These undesirable effects can reach intolerable magnitudes, especially when the ASIC 114 is a high frequency device such as a device with a clock frequency of 1 gigahertz or more.

Please replace the paragraph on page 8, line 6 as follows:

Fig. 6 illustrates another embodiment of the present invention in which some or all balls 612 of a termination board ball grid array 614 are aligned with vias [666] 616 of the main PCB 618 which receives column columns 622 of a column grid array ASIC 624.

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